

22. The computer system of claim 21, wherein each slice includes at least one macroblock.

23. The computer system of claim 22, wherein said video is encoded in MPEG standard.

24. The computer system of claim 23, wherein system computer system decodes said video in real-time.

REMARKS

The foregoing amendment and the following arguments are provided to impart precision to the claims, by more particularly pointing out the invention, rather than to avoid prior art.

Claims 2, 10, and 18 have been canceled. Claims 1, 3-9, 11-17, and 19-24 remain pending.

35 U.S.C. § 102(b) Rejections

Examiner rejected claims 1-24 under 35 U.S.C. §102(b) as obvious by Andrew, et al., U.S. Patent No. 5,428,403 (hereinafter referred to as "Andrew").

"To anticipate a claims, the reference must teach every element of the claim. A claim is anticipated only if each and every element as

set forth in the claim is found, either expressly or inherently described, in a single prior art reference." (Manual of Patent Examining Procedures (MPEP) ¶ 2131.)

Independent claims 1, 9, and 17 of the present application includes limitations not disclosed or taught by the Andrew. As a result, claims 1, 9, and 17 are not anticipated by the Andrew.

In particular, the independent claims include the limitation of assigning at least one slice per processor (in a set a of processors) to be decoded by the processors in parallel. Andrew, however, does not disclose assigning at least one slice per processor (in a set a of processors) to be decoded by the processors in parallel.

Specifically, Andrew only discloses: "blocks are divided into their horizontal rows, and all the blocks of a row are processed, in left to right, by a single DSP". As a result, Andrew fails to disclose assigning "slices" and also fails to disclose assigning slices to multiple processors to be decoded in parallel, as claimed by applicant. Rather, Andrew discloses assigning to "a single DSP" to process "blocks" sequentially.

In addition, Andrew would not be modified to disclose the distinguishing claim limitations because there is no suggestion found in Andrew to modify the disclosure in Andrew to disclose the distinguishing claim limitations. "The mere fact that references can be combined or

modified does not render the resultant combination obvious unless the prior art also suggest the desirability of the combination." *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990); MPEP 2143.01.

The remaining claims depend from one of claims 1, 9, and 17. As a result, the remaining claims include the distinguishing claim limitation discussed above and are therefore not anticipated by Andrew.

CONCLUSION

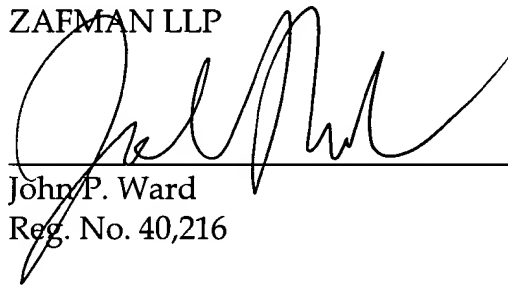
Applicants respectfully submit the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call John Ward at (408) 720-8300, x237.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

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A handwritten signature in black ink, appearing to read 'John P. Ward', is written over a horizontal line.

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ATTACHMENT A

A marked-up version of the amended claims is as follows:

(Once Amended) 1. A method for decoding compressed video comprising:

reading a stream of compressed video into a memory, said video having multiple pictures, each picture having one or more independent [elements] slices;

assigning, via a first processor of a group of processors sharing said memory, at least one independent [element] slice per processor to be decoded by the processors in parallel; and

decoding the independent elements of the video in parallel.

2. (Canceled)

(Once Amended) 3. The method of claim [2] 1, wherein assigning the independent elements includes assigning a varying number of slices to individual processors.

4. The method of claim 3, wherein assigning the independent elements includes assigning a comparable work load to the processors.

5. The method of claim 4, wherein assigning the independent elements includes placing in memory as a local variable, for each processor, the slices to be decoded by a respective processor.

6. The method of claim 5, wherein each slice includes at least one macroblock.

7. The method of claim 6, wherein said video is encoded in MPEG.

8. The method of claim 7, wherein the method of decoding is performed in real-time.

(Once Amended) 9. A computer-readable medium having stored thereon a set of instructions, said set of instruction for decoding compressed video, which when executed by a processor, cause said processor to perform a method comprising:

reading a stream of compressed video into a memory, said video having multiple pictures, each picture having one or more independent [elements] slices;

assigning, via a first processor of a group of processors sharing said memory, at least one independent slice [element] per processor to be decoded by the processors in parallel; and

decoding the independent elements of the video in parallel.

10. (Canceled)

(Once Amended) 11. The computer-readable medium of claim [10] 9, wherein assigning the independent elements includes assigning a varying number of slices to individual processors.

12. The computer-readable medium of claim 11, wherein assigning the independent elements includes assigning a comparable work load to the processors.

13. The computer-readable medium of claim 12, wherein assigning the independent elements includes placing in memory as a local variable, for each processor, the slices to be decoded by a respective processor.

14. The computer-readable medium of claim 13, wherein each slice includes at least one macroblock.

15. The computer-readable medium of claim 14, wherein said video is encoded in MPEG standard.

16. The computer-readable medium of claim 15, wherein the method of decoding is performed in real-time.

(Once Amended) 17. A computer system comprising:

a plurality of processors ;
a memory coupled to said plurality of processors;
a first unit of logic to read a stream of compressed video into said memory, said video having multiple pictures, with each picture having one or more independent [elements] slices; and
said first unit of logic further assigns, via a first processor of said group of processors sharing said memory, at least one independent [element] slice per processor to be decoded by the processors in parallel.

18. (Canceled)

(Once Amended) 19. The computer system of claim [18] 19, wherein said first unit of logic assigns a varying number of slices to individual processors.

20. The computer system of claim 19, wherein said first unit of logic assigns a comparable work load to the processors.

21. The computer system of claim 20, wherein said first unit of logic places in memory as a local variable, for each processor, the slices to be decoded by a respective processor.

22. The computer system of claim 21, wherein each slice includes at least one macroblock.

23. The computer system of claim 22, wherein said video is encoded in MPEG standard.

24. The computer system of claim 23, wherein system computer system decodes said video in real-time.